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AEROFLEX COLORADO SPRINGS, INC.
9

10 UNITED STATES DISTRICT COURT
11 NORTHERN DISTRICT OF CALIFORNIA
12 SAN FRANCISCO DIVISION

13 RICOH COMPANY, LTD.,
14

15 Plaintiff,

16 vs.

17 AEROFLEX INCORPORATED, AMI
SEMICONDUCTOR, INC., MATROX
18 ELECTRONIC SYSTEMS LTD., MATROX
GRAPHICS INC., MATROX
INTERNATIONAL CORP., MATROX TECH,
19 INC., AND AEROFLEX COLORADO
SPRINGS, INC.
20

21 Defendants.

22 SYNOPSIS, INC.,
23

24 Plaintiff,

25 vs.

26 RICOH COMPANY, LTD.,
27

28 Defendant.

Case No. C03-04669 MJJ (EMC)

Case No. C03-02289 MJJ (EMC)

**NOTICE OF MOTION AND MOTION FOR
SUMMARY JUDGMENT OF NON-
INFRINGEMENT (RTL)**

[SUMMARY JUDGMENT MOTION NO. 1]

Date: September 26, 2006
Time: 9:30 a.m.
Courtroom: 11, 19th Floor
Judge: Martin J. Jenkins

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NOTICE OF MOTION AND MOTION

PLEASE TAKE NOTICE that on September 26, 2006, at 9:30 a.m., before the Honorable Martin J. Jenkins in Courtroom 11, 19th Floor, in the United States District Court, 450 Golden Gate Avenue, San Francisco, California, Plaintiff Synopsys, Inc. ("Synopsys") and Defendants Aeroflex Incorporated, Aeroflex Colorado Springs, Inc., AMI Semiconductor, Inc., Matrox Electronic Systems Ltd., Matrox Graphics Inc., Matrox International Corp., and Matrox Tech, Inc. ("the Customer Defendants") will move for summary judgment pursuant to Rule 56 of the Federal Rules of Civil Procedure that the Customer Defendants do not infringe claims 13-17 of U.S. Patent No. 4,922,432 ("the '432 patent") and for Declaratory Relief that the Synopsys Design Compiler system is not capable of infringing the asserted claims. This motion is based on the memorandum of points and authorities set forth below, the accompanying declarations, exhibits, and proposed order, the oral arguments of counsel at the hearing on this motion, and all other pleadings and matters of record in these actions.

MEMORANDUM OF POINTS AND AUTHORITIES

I. INTRODUCTION

The amount of discovery that Ricoh has obtained from Synopsys and the Customer Defendants in this litigation is staggering and mind-boggling: over 12 millions pages of documents, 240 hours of depositions, and full access to Synopsys' accused Design Compiler software source code. Yet despite this wealth of information at its fingertips, Ricoh still cannot come up with any coherent theory of infringement against the Customer Defendants. Ricoh alleges that the Customer Defendants infringe the '432 patent by designing application specific integrated circuits ("ASICs") using Synopsys' Design Compiler system, and has accused over 350 Customer Defendant designs made through this allegedly infringing process.

As the Court is aware, Ricoh began demanding this massive discovery at the Case Management Conferences last summer. Ricoh insisted that it needed significant information – and a deposition – about each ASIC for which any portion of the design was created using the Design Compiler system. Millions of dollars have been wasted responding to this discovery. But it is obvious from the bare-

1 bones expert reports recently submitted by Ricoh's infringement experts that Ricoh has no real
 2 evidence to support these allegations. Indeed, on June 23, 2006, Ricoh served six infringement expert
 3 reports – three from Dr. Donald Soderman (one each for Aeroflex, Matrox, and AMI), and three from
 4 Dr. Marios Papaefthymiou (one each for Aeroflex, Matrox, and AMI). [Exs. 9 and 11]. The three
 5 reports of Dr. Soderman are virtually identical to one another, with only minor variations depending on
 6 the Customer Defendant. The same is true for the three reports of Dr. Papaefthymiou.¹ The Soderman
 7 report is 36 double-spaced pages; of which the first 8 pages are just background; the Papaefthymiou
 8 report is 16 double spaced pages.

9 Ricoh's most egregious error is its failure to apply the Court's construction of a critical term in
 10 the asserted '432 patent claims: "architecture independent actions and conditions." The Court ruled
 11 that the patentee disclaimed *all register-transfer-level descriptions* ("RTL descriptions") during
 12 prosecution of the patent application for the '432 patent, as follows:

13 The '435 patent specifically defines a register-transfer level description and the
 14 subsequent translation or transformation steps described in that patent do not alter this
 15 explicit definition. . . . [A]n examination of the '432 patent's public record fails to
 16 provide any support for Ricoh's distinction between "structural" and "functional" RTL-
 17 type input systems. Given these findings, Ricoh's attempt to limit the patentee's
 disclaimer to only "structural" level RTL-type input systems is unpersuasive. . . .
 Accordingly, *the prosecution history indicates that the patentee expressly disclaimed all*
register-transfer level descriptions.

18 Given these considerations, the Court defines "architecture independent actions and
 19 conditions" as *functional or behavioral aspects of a portion of a circuit (or circuit*
segment) that does not imply a set architecture, structure, or implementing technology,
 20 *but excludes the use of register-transfer level descriptions as taught in Darringer.* Ex. 8
 at 12:5-14 (first emphasis added).

21 Notwithstanding what is a clear ruling, Ricoh's alleged expert on "architecture independent actions and
 22 conditions" expressly acknowledges he has not analyzed whether the input to the Design Compiler
 23 system is RTL at all:

24 Q As you sit here today, do you have an opinion about whether or
 not the customer designs at issue in this litigation are structural RTL?

26 ¹ Because the reports are virtually identical, page and line citations to the reports herein will be limited to the reports
 27 pertaining to the Aeroflex entities (Exs. 9A and 11A). Unless otherwise noted, all exhibits referenced in this motion are
 28 attached to the Declaration of Denise M. De Mory In Support of Synopsys' and Customer Defendants' Summary Judgment
 Motions filed concurrently herewith. All deposition references are likewise included in the De Mory Declaration.

1 A I was not asked to formulate an opinion about that.

2 Q. And therefore you have no opinion about that; is that correct?

3 A. At this point, I have not considered the question.

4 Q. And the same is true with regard to the functional RTL question,
5 just so that the record's clear. As you sit here today, you've not been asked to
6 formulate an opinion about whether or not the customer designs at issue in this
litigation are functional RTL, and therefore you have no opinion on that as you
sit here today?

7 A. That is correct. At this point I have not formulated an opinion about that.

8 Ex. 11 (Papaefthymiou) at 44:4-22.

9 Instead Dr. Papaefthymiou advances the same exact arguments Ricoh already made, and that
10 this Court already rejected, that Darringer RTL is some special breed of RTL as evidenced by a
11 comparison of Dr. Papaefthymiou's opinions regarding "Darringer" RTL with the Court's claim
12 construction ruling:

13 What Dr. Papaefthymiou Says In His Expert 14 Report Regarding Why The Inputs Are Not "Darringer RTL"	15 What the Court's Claim Construction Order Says
16 "In my opinion, the Darringer Patent uses the 17 term 'RTL' in the sense of the older (then- 18 prevalent) structural RTL that is not claimed by 19 the '432 patent. Ex. 9A at 13:6-8.	20 "[A]n examination of the '432 patent's public 21 record fails to provide any support for Ricoh's 22 distinction between 'structural' and 'functional' 23 RTL-type input systems. Given these findings, 24 Ricoh's attempt to limit the patentee's 25 disclaimer to only 'structural' level RTL-type input systems is unpersuasive." Ex. 9 at 12:9- 12.
26 "That the RTL used in the Darringer Patent 27 closely describes the architecture of the hardware 28 desired in the design is evident from the requirement in the Darringer Patent that the inputs undergo a simple translation of the specification into equivalent AND/OR logic." Ex. 9A at 13:13-17.	29 "The '435 patent specifically defines a register- transfer level description and the subsequent translation or transformation steps described in that patent do not alter this explicit definition." Ex. 9 at 12:5-7.

30 Thus, because Ricoh's expert on "architecture independent actions and conditions" has offered
31 no opinion regarding the Court's definition of this term in their infringement analyses, those analyses
32 must be completely rejected. And, this is not a close call. Ricoh ignored the express rulings of the

1 Court that Ricoh knows should have ended this case at least as early as April of 2007 when the Court
2 issued its Claim Construction Order.

3 It gets worse. Ricoh's other expert, Dr. Soderman, who offered opinions on all other technical
4 issues, including all technical infringement, enforceability, and validity issues, testified at deposition
5 that the customer designs meet the "explicit definition" of Darringer. Indeed, Dr. Soderman was the
6 author of several papers and a patent in which he made affirmative statements about RTL that directly
7 refute Ricoh's claims in this case. And, there is no doubt about this issue, as set forth in the Casavant
8 declaration, confirmed by Dr. Soderman's testimony - the inputs are not "architecture independent"
9 and are RTL.

10 Because Ricoh will not be able to prove at trial that the Customer Defendants meet every single
11 element of the asserted claims, as a matter of law, the Court should grant summary judgment of non-
12 infringement with respect to all of the asserted claims and all of the accused Customer Defendant
13 designs. In addition, because it is obvious that the Synopsys tools are not capable of infringing the
14 asserted patent, summary judgment should be granted in favor of Synopsys on its declaratory
15 noninfringement claim.²

16 **II. STATEMENT OF FACTS**

17 Ricoh alleges that the Customer Defendants infringe claims 13-17 of the '432 patent by
18 designing ASICs using Synopsys' software tools. The '432 patent relates generally to a computer-
19 aided design system for designing ASICs in which a user inputs a description of the desired functions
20 for the ASIC into the design system, which then translates the description into a "netlist" of the
21 hardware cells required to implement the desired functions of the ASIC.

22
23
24
25
26 ² Synopsys and the Customer Defendants have also filed concurrently two other Motions for Summary Judgment of Non-
27 Infringement, which present other bases upon which this Court can find summary judgment of non-infringement. Synopsys
28 and the Customer Defendants believe, however, that the arguments presented in the present Motion alone are sufficient to
establish non-infringement.

1 Claim 13 of the '432 patent is the only independent claim asserted by Ricoh.³ The text of
 2 Claim 13 reads, in relevant part:

3 A computer-aided design process for designing an application specific integrated circuit
 4 which will perform a desired function comprising:

5 describing for a proposed application specific integrated circuit *a series of architecture
 independent actions and conditions*;

6 The “describing” step at issue requires that the proposed ASIC be described by a series of
 7 “*architecture independent* actions and conditions.”

8 During prosecution of the '432 patent, the patentee added the term “architecture independent”
 9 to the '432 patent claims in order to distinguish the claimed invention over prior art, including U.S.
 10 Patent No. 4,703,435 issued to Darringer et al. (“Darringer”) *See* Ex. 7 at 34-35; Ex. 15 at 9; Ex. 16 at
 11 7. Darringer et al. discloses a computer-aided design system for designing ASICs in which the user
 12 inputs a specification for the ASIC in a format called register-transfer level, or “RTL.” The '432
 13 patentee argued to the patent examiner that the additional term “architecture independent”
 14 distinguished his invention from Darringer’s because “the specifications used by Darringer et al. are
 15 not truly at an architecture independent level, but rather are at a lower level which is indeed hardware
 16 architecture dependent and defines the system at a ‘register-transfer’ level description. Ex. 16 at 7
 17 (emphasis in original). The Customer Defendants and Synopsys argued at claim construction that this
 18 statement showed that the '432 patentee intended to exclude all types of RTL descriptions from the
 19 scope of the '432 patent claims. Ex. 7 at 34-35.

20 Ricoh, however, tried to argue that Darringer et al. discloses the use of only a “primitive” or
 21 “structural” type of RTL, as opposed to more “functional” types of RTL such as VHDL and Verilog.
 22 Ex. 5 at 21:3-17; Ex. 7 at 8:6-10. Ricoh asserted that the patentee’s statement about Darringer
 23 therefore should be interpreted as a disclaimer of only the “primitive/structural” type of RTL. *Id.*
 24 Specifically, Ricoh argued that “to the extent it is necessary to clarify what is excluded from the proper
 25

26 _____
 27 ³ Claims 14-17 are dependent on claim 13. Thus, if claim 13 is not infringed, then claims 14-17 also are not infringed. *See*
 28 *Wahpeton Canvas Co., Inc. v. Frontier, Inc.*, 870 F.2d 1546, 1552 n.9 (Fed. Cir. 1989) (“One who does not infringe an
 independent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim.”).

1 interpretation of the term ‘architecture independent actions and conditions,’ the exclusion should be
 2 limited to ‘basic’ or ‘primitive RTL-type descriptions’ and not the entire category of ‘RTL’
 3 descriptions, as contended by Defendants.” *Id.* at 21:14-17.

4 The Court rejected Ricoh’s argument and essentially agreed with the Customer Defendants’
 5 and Synopsys’ interpretation, stating in its April 7, 2005 Claim Construction Order that:

6 [A]n examination of the ’432 patent’s public record fails to provide any support for
 7 Ricoh’s distinction between “structural” and “functional” RTL-type input systems.
 8 Given these findings, Ricoh’s attempt to limit the patentee’s disclaimer to only
 9 “structural” level RTL-type input systems is unpersuasive. . . . Accordingly, the
 10 prosecution history indicates that the patentee expressly disclaimed all register-transfer
 11 level descriptions.

12 Given these considerations, the Court defines “architecture independent actions and
 13 conditions” as *functional or behavioral aspects of a portion of a circuit (or circuit
 14 segment) that does not imply a set architecture, structure, or implementing technology,
 15 but excludes the use of register-transfer level descriptions as taught in Darringer.*

16 [Ex. 8 at 12:9-19] (emphasis in original).

17 As for what is a “register-transfer level description as taught in Darringer,” the Court stated that
 18 “[t]he ’435 patent *specifically defines* a register-transfer level description and the subsequent
 19 translation or transformation steps described in that patent do not alter this *explicit definition.*” Ex. 8
 20 at 12:5-7 (emphasis added). The Court’s footnote 7, following this passage, points to the definition of
 21 RTL set forth in the Darringer patent as follows:

22 [T]he process of this invention begins at step 100 with a register-transfer level
 23 description, e.g. of the type shown in Fig. 4. The description consists of two parts: a
 24 specification of the inputs, outputs and latches of the chip to be synthesized; and a
 25 flowchart-like specification of control, describing for a single clock cycle of the
 26 machine how the chip outputs and latches are set according to the values of the chip
 27 inputs and previous values of the latches. At step 102 in FIG 2, the register-transfer
 28 level description undergoes a simple translation to an initial implementation of
 AND/OR logic. ’435 patent, col. 5:27-38.

[Ex 8 at 12 n.7].

On March 24, 2006, Ricoh served its Final Infringement Contentions. (*See* Ex. 4) Those
 contentions, as described above, cite to papers that confirm that the inputs used by the Customer
 Defendants to “describe” their ASICs are RTL. In addition to the documents quoted above, also
 quoted by Ricoh in their Final Infringement Contentions, the following documents also indicate that
 the inputs are RTL:

- MGI 0033893 at ¶ 1: “Your success with Design Compiler is directly related to your RTL code and how it interacts with DC.”
- MGI 0033900 at ¶ 1.5.1: “Think of synthesis as refining (or polishing) what you started (with your RTL description).”
- MGI 0033903 at second column: “The functionality of generic flip-flops [i.e., latches] is defined by sequential logic description in your RTL.”
- RCL011421-22: “If you remember back when Synopsys first came out with their Design Compiler (DC) tool, we slowly learned that we could be more productive ASIC designers by writing Synopsys compatible **VHDL RTL code** and inferring gates instead of instantiating gates with a schematic capture tool.” (emphasis added)
- SP 0167847: “DC Ultra is the best-in-class, industry leading RTL Synthesis solution for today’s challenging designs . . . ”
- SP 0167849: “DC Ultra now allows for automatic extraction and optimization of Finite State Machines (FSMs) from the **RTL code** for the purpose of optimizing the state assignment. This feature is supported **for both Verilog and VHDL.**” (emphasis added)
- SP59897: “The **register transfer level** completely models your design in detail. All clocks are defined and all registers declared. *Use this HDL model as input for Design Compiler.*” (italics added)
- SP59968: (Presentation slide showing that Design Compiler optimizes logic in RTL code.)

Ex. 4 at 13-16.

Additionally, several presentation charts cited in Ricoh’s Final Infringement Contentions show RTL as the direct input to Synopsys’ HDL Compiler (or “Presto”). See Ex. 4 at 13-16 (citing SP 0167849; SP 0167852; SP 0168745; SP 0168746; SP 0168748; SP 0168750; SP 0168752; MGI 0001490; and SP59897). Finally, the deposition testimony cited in Ricoh’s Final Contentions also unambiguously state that RTL is the input to Design Compiler. See Ex. 4 at 16 (citing David Tran Dep., Vol. 1 at 19:6-7 (“the language, a hardware description language that the tools support is RTL.”); Shir-Shen Chang Dep. at 54:1-3 (“For Design Compiler, we use all kinds of input, including the RTL level of the abstraction.”); Karen Pieper Dep. at 14:22-23 (“Q: What did you mean by [synthesis]? A: Translating input RTL to unmapped gates.”)). All of these documents cited in Ricoh’s Infringement Contentions clearly show that RTL is the input to Design Compiler and that VHDL and Verilog are considered RTL.

1 As with its infringement contentions, Ricoh's Expert reports are premised first and most
 2 fundamentally on the notion that: (1) the Court did not rule that all RTL is excluded, but rather there is
 3 some non-disclaimed/non-Darringer RTL; (2) the test for whether or not something falls into the
 4 category of non-disclaimed/non-Darringer RTL is whether the inputs undergo a simple translation, or
 5 not finally based solely by looking at whether or not the inputs contain VHDL or Verilog HDL
 6 operators such as + or -.⁴ Notably, they do not analyze whether the designs contain a specification of
 7 inputs, outputs, and latches, or any information about control as to how the outputs and latches are set,
 8 or whether the designs are "architecture independent."

9 On August 14, Dr. Papaefthymiou was deposed. Although his report indicates that RTL can be
 10 structural or functional RTL, he made no effort to determine whether or not the Customer Defendant
 11 designs were either structural or functional RTL, as discussed above. Ex. 11 (Papaefthymiou) at 44:4-
 12 22. Thus, even though Dr. Papaefthymiou is the alleged "architecture independent" expert, he made
 13 no effort to determine if the customer designs were or were not RTL *of any variety*. In fact, he didn't
 14 even ever have physical possession of the designs and only looked at some over a Web-Ex connection.

15 Dr. Soderman, for his part, clearly admitted that the designs *were* RTL, and, leaving aside the
 16 already rejected "simple translation issue," admitted that the Customer Defendant designs met all the
 17 elements of the definition of Darringer cited by the Court as the "explicit definition." Darringer
 18 defines RTL as containing two parts: a specification of the inputs, outputs and latches of the chip to be
 19 synthesized; and a flowchart-like specification of control, describing for a single clock cycle of the
 20 machine how the chip outputs and latches are set according to the values of the chip inputs and
 21 previous values of the latches." Ex. 22 at 5:9-25. Dr. Soderman testified as follows:

22 Q: Do the customer designs include a specification of the inputs?
 23 _____

24 ⁴ Separate and apart from the merits of this motion, this fact alone demonstrates the severe abuse of process in which Ricoh
 25 has engaged. Ricoh insisted both that it had to have every input and output for every product designed using Design
 26 Compiler by the Customer Defendants (some 400 in total resulting in the expensive production of millions of pages of
 27 documents) as well as deposition testimony on each of the products – well over 100 hours of testimony. Then, after
 28 insisting on this discovery that cost MILLIONS, Ricoh's whole infringement theory is premised on the notion that the
 designs contain at least one + or -. Ricoh didn't need discovery for this – all they had to do was buy an HDL synthesis
 book, or talk to its own engineers who have been using Design Compiler for over 15 years. This too makes this case
 exceptional.

1 A: Yes.

2 Q: Do the customer Defendant designs include a specification of the outputs?

3 A: Yes.

4 Ex. 13 (Soderman) at 77:21-78:1.

5 Q: Let's do it this way. Do the customer Defendant designs include a specification of
6 FlipFlops⁵ if we define specification of FlipFlops to include inferring if FlipFlop from
7 statements such as always@(posclkgedge)?

8 A: Yes.

9 Ex. 13 (Soderman) at 108:2-9.

10 Q: Let me try it again. Do the customer Defendant designs include for each clock cycle a
11 description of how the values of the outputs and FlipFlops should be set according to the values
12 of the inputs, the previous values of the FlipFlops and the logic functionality as specified by
13 the HDL operators?

14 A: Yes.

15 Ex. 13 (Soderman) at 80:1-13.

16 Moreover, Dr. Soderman admitted that Design Compiler has long required RTL input:

17 Q: So let's make these specific, these questions specific to Design Compiler. In 1997 – so
18 I'll go back a little bit, just so we have the record clear. In 1997, a compiler like Design
19 Compiler needed information about what the inputs and outputs were going to be; is that
20 correct?

21 A: Yes.

22 Q: In 1997, a compiler like Design Compiler needed information about the cycle-by-cycle
23 characteristics or behavior of the circuit; is that correct?

24 A: Indeed in some of those functional descriptions, yes.

25

26 ⁵ Latches and flip-flops are both memory elements, or registers. Dr. Soderman testified that in the case of the Customer
27 Defendant designs, the customers used flip-flops as the register elements. Indeed, the fact that Dr. Soderman can determine
28 this from the input totally undercuts Ricoh's argument about "architecture independent." Indeed, Dr. Soderman testified
that always@(posclkgedge) infers a positive edge triggered flip-flop.

1 Q: Did it need information on timing, or how things performed on a clock-by-clock cycle
2 basis?

3 A: That was additional information that was put in.

4 Ex. 13 (Soderman) at 19:14-20:5.

5 Thus, based on this testimony, whether you call it RTL or not, it is clear that the inputs to Design
6 Compiler are not and always were not “architecture independent.”⁶ Notably, the Court construed
7 “architecture independent actions and conditions” as *functional or behavioral aspects of a portion of a*
8 *circuit (or circuit segment) that does not imply a set architecture, structure, or implementing*
9 *technology, but excludes the use of register-transfer level descriptions as taught in Darringer.”* [Ex. 8
10 at 12:17-19] Dr. Soderman acknowledges that the inputs for “each portion of a circuit (or circuit
11 element)” that are input into Design Compiler do imply a set architecture. He testified that the inputs,
12 outputs, latches, control, and how the values of the outputs and latches are set based on the value of the
13 inputs and the previous values of the latches is all specified in the Customer Defendant designs. Ex. 13
14 (Soderman) 89:14-90:5. This architecture of the circuit must be set in advance to design an ASIC
15 using the Design Compiler system. Thus, Ricoh’s semantic games regarding “RTL” aside, the input to
16 the Design Compiler system for the Customer Defendants (and in fact, all users) is not and has always
17 been not “architecture independent.” See Casavant Declaration at ¶¶ 37-48.

18 Unlike Ricoh’s purely litigation inspired theory and highly suspect claim that there is
19 infringement based on its claim that the meaning of RTL has changed over time, documents dating
20 back to at least 1991 (and indeed earlier) make clear that the inputs to the Design Compiler system are
21 both RTL and architecture dependent. For example, a book authored by then Synopsys employee
22

23
24 ⁶ Indeed, Dr. Soderman represented to the United States Patent & Trademark Office in 1997 that RTL is the expected input
25 to synthesis tools. The invention disclosed in Dr. Soderman’s U.S. Patent No. 6,226,776 “converts the preliminary
26 hardware design to a register transfer level HDL, which enables the HDL design to be synthesized.” Ex. 18 at 4:42-44. In a
27 1998 paper entitled “Implementing C Algorithms in Reconfigurable Hardware using C2Verilog,” Dr. Soderman states that
28 “the compiled RTL Verilog can then be synthesized using any one of a number of products from Synopsys...” Ex. 20.
Discussing a weakness of a prior art method to the ‘776 patent, Dr. Soderman states: “Design output...can be in so-called
“behavioral HDL” which in many cases cannot be synthesized by existing synthesis programs into a gate-level
representation of the hardware. The system in accordance with the invention generates register transfer level HDL that can
always be synthesized.” Ex. 18 at 27:15-20.

Steve Carlson and published by Synopsys in 1991 entitled “Introduction to HDL-Based Design Using Verilog” (“1991 Synopsys VHDL Reference”) is completely consistent with Synopsys’ and the Customer Defendants’ position in this litigation. Specifically, the 1991 Synopsys VHDL Reference describes the inputs as follows:

The input to HDL synthesis is an RTL (register transfer level) functional description of the network to be implemented. RTL descriptions are distinct from behavioral level descriptions. The distinction is that *a behavioral description has no implied architecture in its representation, while an RTL level description has a definite, implied architecture.*

Ex. 21 at 3 (emphasis in original). The 1991 Synopsys VHDL Reference also describes the design methodology for the HDL design process, starting with the RTL description. The 1991 VHDL Book describes this process as follows:

The HDL design process begins with the development of an RTL level functional description of the network to be implemented. The process of creating the RTL network description is often a two-tiered approach. The first steps involve a top-down architectural definition where all of the major functional units of the design are defined, and at a top level hierarchy is created. These units are typically ALU’s, RAM, ROM, or data paths. The second steps are a bottom-up, or middle-up, functional description-creation process. In these steps, the source HDL describes the functional behavior characteristics of each of the architecture units at an RTL level.

Ex. 21 at 8; see also Casavant Declaration at ¶ 48. Simply put, there is no doubt that the input for the entire design, and each circuit element or circuit segment, is defined, at a register transfer architecture dependent level in the Customer Defendants’ designs. Indeed, this is how the Design Compiler system works, and has worked, since it was introduced. Ironically (and tragically in terms of the wasted resources on this case) Ricoh knows this, and has known this since 1990, when Ricoh first began licensing and using the accused Design Compiler system. *See, e.g.* Motion No. 8 (seeking summary judgment of laches).

III. ARGUMENT

A. Legal Standard

Summary judgment is proper “if the pleadings, depositions, answers to interrogatories and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to a judgment as a matter of law.” Fed. R. Civ. P. 56(c). In the context of a patent case, this means that an accused infringer seeking summary judgment

1 of non-infringement may meet its initial responsibility either by providing evidence that would
 2 preclude a finding of infringement, or by showing that the evidence on file fails to establish a material
 3 issue of fact essential to the patentee's case. *See Novartis Corp. v. Ben Venue*, 271 F.3d 1043, 1046,
 4 1050-51, 1055 (Fed. Cir. 2001). Once the moving party makes this initial showing, the burden shifts to
 5 the non-moving party to "designate specific facts showing that there is a genuine issue for trial."
 6 *Celotex Corp. v. Catrett*, 477 U.S. 317, 324 (1986) (citation omitted); *Aguilera v. Pirelli Armstrong*
 7 *Tire Corp.*, 223 F.3d 1010, 1019 (9th Cir. 2000) (citation omitted) ("On a motion for summary
 8 judgment, the non-moving party cannot simply rest on its allegations without any significant probative
 9 evidence tending to support the complaint").

10 Determining whether a patent claim has been infringed involves two steps: (1) claim
 11 construction to determine the scope of the claims, followed by (2) determination of whether the
 12 properly construed claim encompasses the accused devices. *Vitronics v. Conceptronic, Inc.*, 90 F.3d
 13 1576, 1581-82 (Fed. Cir. 1996). Literal infringement requires that the patentee prove that the accused
 14 product or process meets every element or limitation of a claim. *Rohm and Haas Co. v. Brotech Corp.*,
 15 127 F.3d 1089, 1092 (Fed. Cir. 1997). If even one element or limitation is missing or is not met as
 16 claimed, then there is no literal infringement. *See Mas-Hamilton Group v. LaGard, Inc.*, 156 F.3d
 17 1206, 1211 (Fed. Cir. 1998); *see also Lantech, Inc. v. Keip Mach. Co.*, 32 F.3d 542, 547 (Fed. Cir.
 18 1994) ("For literal infringement, each limitation of the claim must be met by the accused device
 19 exactly, any deviation from the claim precluding a finding of infringement."). Summary judgment of
 20 no literal infringement is appropriate when no reasonable jury could find every limitation recited in an
 21 asserted claim is found exactly in the accused device. *See Johnston v. IVAC Corp.*, 885 F.2d 1574,
 22 1576-80 (Fed. Cir. 1989).

23 **B. The Customer Defendants' Input Descriptions Do Not Meet Element D of Claim**
 24 **13 Because They Are Not Descriptions of "Architecture Independent Actions and**
 25 **Conditions."**

26 Element D of claim 13 requires "describing for a proposed application specific integrated
 27 circuit a series of architecture independent actions and conditions." Ex. 1, '432 patent, col. 16:45-47.
 28 Ricoh's expert, Dr. Soderman, asserts that the Customer Defendants met element D when they

1 “entered a written description of the desired functions of each ASIC Product into [Synopsys’] HDL
2 Compiler.” Ex. 11A at 24:11-12. According to Dr. Soderman, this written description “was written in
3 a high-level design language (an HDL such as VHDL or Verilog).” *Id.* at 24:12-13. As the language
4 of element D indicates, in order to prove that the Customer Defendants’ accused VHDL and Verilog
5 descriptions meet element D, Ricoh must establish that these descriptions are of “architecture
6 independent actions and conditions.”

7 As discussed below, Ricoh cannot do so because Ricoh concedes that the Customer
8 Defendants’ VHDL and Verilog descriptions constitute RTL descriptions, which the Court already
9 determined are excluded from the term “architecture independent actions and conditions.” Moreover,
10 even if the Court’s Claim Construction Order is read to exclude only “RTL as taught in Darringer,” as
11 Ricoh appears to argue, the Customer Defendants’ accused descriptions also constitute “RTL as taught
12 in Darringer,” and are, regardless of the label, not “architecture independent” inputs. Therefore, the
13 Customer Defendant inputs cannot constitute descriptions of “architecture independent actions and
14 conditions.”

15 **1. The Court’s Claim Construction Order Excludes All RTL from the Scope** 16 **of Claim 13.**

17 In their claim construction brief, Synopsys and the Customer Defendants argued that the
18 prosecution history of the ’432 patent sheds light on the meaning of the phrase “architecture
19 independent actions and conditions.” During prosecution of the ’432 patent, the patentee added the
20 term “architecture independent” to the ’432 patent claims in order to distinguish the claimed invention
21 over prior art, including Darringer et al. *See* Ex. 6 at 34-35; Ex. 40, April 1989 Amendment at 9, and
22 November 1989 Amendment at 7. Darringer et al. discloses a CAD system for designing ASICs in
23 which the user inputs a specification for the ASIC in a format called register-transfer level, or “RTL.”
24 The ’432 patentee argued to the patent examiner that the additional term “architecture independent”
25 distinguished his invention from Darringer’s because “the specifications used by Darringer et al. are
26 not truly at an architecture independent level, but rather are at a lower level which is indeed hardware
27 architecture dependent and defines the system at a ‘register-transfer’ level description. Ex. 40, Nov.
28 1989 Amendment at 7 (emphasis in original). The Customer Defendants and Synopsys argued that this

statement showed that the '432 patentee intended to exclude all types of RTL descriptions from the scope of the '432 patent claims. Ex. 6 at 34-35.

Ricoh, however, tried to argue that Darringer et al. discloses the use of only a "primitive" or "structural" type of RTL, as opposed to more "functional" types of RTL such as VHDL and Verilog. Ex. 5 at 21:3-17; Ex. 7 at 8:6-10]. Ricoh asserted that the patentee's statement about Darringer et al. therefore should be interpreted as a disclaimer of only the "primitive/structural" type of RTL. *Id.* Specifically, Ricoh argued that "to the extent it is necessary to clarify what is excluded from the proper interpretation of the term 'architecture independent actions and conditions,' the exclusion should be limited to 'basic' or 'primitive RTL-type descriptions' and not the entire category of 'RTL' descriptions, as contended by Defendants." *Id.* at 21:14-17.

The Court rejected Ricoh's argument and essentially agreed with the Customer Defendants' and Synopsys' interpretation, stating in its Claim Construction Order that:

[A]n examination of the '432 patent's public record fails to provide any support for Ricoh's distinction between "structural" and "functional" RTL-type input systems. Given these findings, Ricoh's attempt to limit the patentee's disclaimer to only "structural" level RTL-type input systems is unpersuasive. . . . Accordingly, the prosecution history indicates that *the patentee expressly disclaimed all register-transfer level descriptions.*

Given these considerations, the Court defines "architecture independent actions and conditions" as functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply a set architecture, structure, or implementing technology, but excludes the use of register-transfer level descriptions as taught in Darringer.

Ex. 8 at 12:9-19 (emphasis added).

The words of the Court in this passage are clear: *all register-transfer level descriptions* were disclaimed by the '432 patentee. Thus, any input descriptions that constitute RTL descriptions do not meet the "architecture independent actions and conditions" requirement of element D.

Ricoh acknowledges that the Customer Defendants' accused inputs into the Design Compiler system are RTL descriptions. This is apparent from Ricoh's Final Infringement Contentions, in which Ricoh not only cites dozens of documents indicating that the inputs are RTL, but also specifically quotes portions of those documents and deposition testimony indicating that the inputs are RTL. *See* Ex. 4 at 13 (alleging that element D was met by Aeroflex when it entered a written description from

the following input file: “AF 285663 (\RTL\rtl_top.v”); 14 (“Synthesis works best (i.e., has the most freedom to try different optimizations) with high level RTL constructs.”); *Id.* at 15 (“[B]ack when Synopsys first came out with their Design Compiler (DC) tool, we slowly learned that we could be more productive ASIC designers by writing Synopsys compatible VHDL RTL code and inferring gates instead of instantiating gates with schematic capture tool.”); *Id.* at 16 (“I am intending RTL to mean a level of abstraction used to describe the circuit”).

Even Ricoh’s expert, Dr. Papaefthymiou, agrees that descriptions written in Verilog and VHDL languages constitute “functional RTL formats.” [Ex. 9A at 7:20-22].⁷ And Ricoh’s experts agree that the Customer Defendants’ accused input descriptions were written in Verilog and VHDL. Ex. 11A at 24:12-14 (The [accused] description was written in a high-level design language (an HDL such as VHDL or Verilog) . . .”); Ex. 9A at 9:6-7 (“In particular, [the Customer Defendants] use[] HDL (i.e., Verilog and VHDL) input specifications . . .”).⁸ Thus, it is undisputed that the Customer Defendants’ accused input descriptions are RTL. But, the Court excluded RTL from the scope of element D; consequently, there is no way that Ricoh can establish that the Customer Defendants meet element D, and there is no infringement.

2. Even if the Court Intended to Exclude Only RTL Descriptions “as Taught in Darringer” from the Scope of Claim 13, the Customer Defendants’ Input Descriptions Constitute Such Descriptions.

Undoubtedly, Ricoh will contend that the Claim Construction Order does not exclude all RTL descriptions from the scope of the ’432 claims, but only RTL descriptions “as taught in Darringer.”

⁷ The fact that Ricoh hired Dr. Papaefthymiou instead of relying on Dr. Soderman evidences a consciousness that Ricoh knew that its argument was unsupportable. First, although Dr. Soderman has been in the ASIC design business since prior to 1990, Ricoh was required to rely on an expert who obtained his Ph.D. in 1993 to opine about how the meaning of RTL has changed so much over time, that one cannot determine what it means without context. Dr. Soderman’s admissions at deposition are also telling: Dr. Papaefthymiou was obviously hired because Dr. Soderman does not and was not going to support the opinion they needed to keep this case going. Finally, Dr. Papaefthymiou was hired because Dr. Soderman submitted a patent application to the USPTO in 1997, and authored many articles, in 1997 and 1998, that flatly contradict Dr. Papaefthymiou’s contention that the definition of RTL has changed over time and one must look at context. In fact, the RTL described in Dr. Soderman’s 1997 patent application and 1998 papers has the same characteristics as the Darringer patent, and both have the same characteristics as the Customer Defendant designs.

⁸ Ricoh also admitted in response to a Request for Admission that the Customer Defendants’ accused input descriptions are all VHDL or Verilog descriptions. Ex. 14 at 4:24-5:1.

Ricoh bases this argument on the Court's construction of "architecture independent actions and conditions" as "functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply a set architecture, structure, or implementing technology, but excludes the use of register-transfer level descriptions as taught in Darringer." Ex. 8 at 12:16-19.

Even assuming that the Court intended to limit what is excluded from the scope of "architecture independent actions and conditions" to RTL that is taught in Darringer, the Customer Defendants' accused input descriptions are in fact RTL descriptions as taught in Darringer. The Court stated in its Claim Construction Order that "[t]he '435 patent *specifically defines* a register-transfer level description and the subsequent translation or transformation steps described in that patent do not alter this *explicit definition*." Ex. 8 at 12:5-7 (emphasis added). The Court's footnote 7 then sets forth the "explicit definition" of RTL in the Darringer patent as follows:

[T]he process of this invention begins at step 100 with a register-transfer level description, e.g. of the type shown in Fig. 4. The description consists of two parts: a specification of the inputs, outputs and latches of the chip to be synthesized; and a flowchart-like specification of control, describing for a single clock cycle of the machine how the chip outputs and latches are set according to the values of the chip inputs and previous values of the latches. At step 102 in FIG 2, the register-transfer level description undergoes a simple translation to an initial implementation of AND/OR logic. '435 patent, col. 5:27-38.

Ex. 8 at 12 n. 7.

As footnote 7 shows, the Court defined "RTL descriptions as taught in Darringer" as consisting of two parts: (1) a specification of the inputs, outputs and latches of the chip to be synthesized, and (2) a flowchart-like specification of control, describing for a single clock cycle of the machine how the chip outputs and latches are set according to the values of the chip inputs and previous values of the latches.

Thus, the critical infringement question for element D is: do the Customer Defendants' accused input descriptions have these two requirements? If they do, then they do not meet the requirements of element D, and cannot infringe claim 13.

Neither of Ricoh's infringement experts addresses this issue in their expert reports. Dr. Soderman merely states that "[f]rom my conversations with Dr. Marios Papaefthymiou and my review of his Expert Report, I understand that the input description [of the Customer Defendants] . . . does not

1 include ‘the use of register-transfer level descriptions as taught in Darringer,’ as defined in the Claim
 2 Construction Order” Ex. 11A at 24:22-26. Thus, Dr. Soderman provides no opinion on the
 3 subject, but rather relies on whatever Dr. Papaefthymiou says in his report. *See* Ex. 13 (Soderman) at
 4 262:10-17 (“I also relied on Marios’s opinion that this – the descriptions as the HDL code written by
 5 the Defendants was different than Darringer. I felt I didn’t need any more than that.”).

6 As for Dr. Papaefthymiou, he concedes that “the Court in this case has construed the claimed
 7 inputs to exclude the use of RTL descriptions as taught in the Darringer Patent.” Ex. 9A at 13:5-6.
 8 But Dr. Papaefthymiou makes the critical error of failing to apply the Court’s two-part definition of
 9 “RTL descriptions as taught in Darringer” in his report. Instead, Dr. Papaefthymiou states that “[i]n
 10 my opinion, the Darringer Patent uses the term ‘RTL’ in the sense of the older (then-prevalent)
 11 structural RTL that is not claimed by the ’432 patent.” *Id.* at 13:6-8. Dr. Papaefthymiou then goes on
 12 to argue that the Customer Defendants’ input descriptions are different than the RTL disclosed in the
 13 Darringer patent because the Customer Defendants’ descriptions do not undergo the “simple
 14 translation” into AND/OR logic that is shown in the Darringer patent. *Id.* at 13-15.

15 Dr. Papaefthymiou’s opinion completely misses the point. First, what Dr. Papaefthymiou
 16 thinks the term “RTL” means in the Darringer patent is ***completely irrelevant***, because the Court in
 17 footnote 7 of the Claim Construction Order ***already defined*** what “RTL” means in the Darringer
 18 patent. Second, even assuming *arguendo* that Dr. Papaefthymiou is correct that the Darringer patent
 19 shows “simple translations” of design descriptions into AND/OR logic, that has nothing to do with
 20 whether or not the Customer Defendants’ input descriptions consist of: (1) a specification of the inputs,
 21 outputs and latches of the chip to be synthesized, and (2) a flowchart-like specification of control,
 22 describing for a single clock cycle of the machine how the chip outputs and latches are set according to
 23 the values of the chip inputs and previous values of the latches – the Court-ordered definition of
 24 Darringer RTL that must be applied.

25 Moreover, a comparison between Dr. Papaefthymiou’s opinions on the definition of RTL with
 26 the Claim Construction Order reveals that Dr. Papaefthymiou’s opinions are nothing more than a
 27 rehash of the arguments Ricoh asserted during claim construction, and which the Court clearly
 28 rejected:

What Dr. Papaefthymiou Says In His Expert Report	What the Court's Claim Construction Order Says
<p>"In my opinion, the Darringer Patent uses the term 'RTL' in the sense of the older (then-prevalent) structural RTL that is not claimed by the '432 patent. Ex. 9A, at 13:6-8.</p>	<p>"[A]n examination of the '432 patent's public record fails to provide any support for Ricoh's distinction between 'structural' and 'functional' RTL-type input systems. Given these findings, Ricoh's attempt to limit the patentee's disclaimer to only 'structural' level RTL-type input systems is unpersuasive." Ex. 8, at 12:9-12.</p>
<p>"That the RTL used in the Darringer Patent closely describes the architecture of the hardware desired in the design is evident from the requirement in the Darringer Patent that the inputs undergo a simple translation of the specification into equivalent AND/OR logic." Ex 9A at 13:13-17.</p>	<p>"The '435 patent specifically defines a register-transfer level description and the subsequent translation or transformation steps described in that patent do not alter this explicit definition." Ex. 8 at 12:5-7.</p>

It is therefore apparent that, instead of applying the Court's "explicit definition" of Darringer RTL to the issue of infringement, Dr. Papaefthymiou tries to argue for the Darringer RTL definition that Ricoh failed to convince the Court to adopt during claim construction.

It is improper for Dr. Papaefthymiou to attempt to reargue the proper construction of "register-transfer level descriptions as taught in Darringer." The Court's claim construction must be faithfully applied to the accused process to determine whether literal infringement exists. *See Searfoss v. Pioneer Consol. Corp.*, 374 F.3d 1142, 1148 (Fed. Cir. 2004) ("Analysis of infringement involves two steps. . . . First, the trial court determines the scope and meaning of the asserted claims. . . . Second, the claims **as construed by the court** are compared limitation by limitation to the features of the allegedly infringing device.") (emphasis added). Dr. Papaefthymiou's infringement opinion is therefore critically flawed with respect to element D.

Dr. Papaefthymiou's opinion is also flawed in another respect. As discussed above, Dr. Papaefthymiou tries to make the distinction that the RTL described in the Darringer patent is "structural RTL." Ex. 9A at 13:6-8; Ex. 10 at 40:21-41:7. Yet he admitted in his deposition that he has formed no opinion as to "whether or not the inputs to the [accused] designs are functional or

1 structural RTL.” Ex. 10 at 180:1-5; 44:4-12. Dr. Papaefthymiou’s logic here makes no sense. If he
 2 believes that the RTL taught in Darringer is “structural RTL,” but he does not know whether or not the
 3 Customer Defendants’ accused input descriptions constitute “structural RTL,” then how can he
 4 possibly know whether or not the accused input descriptions are “RTL descriptions as taught in
 5 Darringer”?

6 The Customer Defendants’ expert, Dr. Casavant, does not make the same analytical mistakes
 7 as Dr. Papaefthymiou. Dr. Casavant addresses the two-part definition of Darringer RTL head-on and
 8 concludes based on his review of exemplary Customer Defendant input descriptions that, indeed, the
 9 Customer Defendants’ input descriptions do meet the two-part definition of Darringer RTL set forth by
 10 the Court. Casavant Decl. at ¶¶ 40 - 42. Dr. Casavant’s opinion is further supported by several
 11 publications – including articles authored by Dr. Soderman himself – indicating that the RTL
 12 description input into the Design Compiler system must have an implied architecture, like the RTL
 13 taught in the Darringer patent. *Id.* at ¶¶ 43 – 48; Ex. 18 – 21. Moreover, as set forth above, Ricoh’s
 14 “other” expert on all other issues, Dr. Soderman, agrees with Dr. Casavant, the inputs meet the
 15 Darringer definition.

16 In light of Ricoh’s failure to provide an expert opinion that applies the correct construction of
 17 element D to the Customer Defendants’ accused input descriptions, Ricoh cannot establish literal
 18 infringement as a matter of law. *See Kemco Sales, Inc. v. Control Papers Co., Inc.*, 208 F.3d 1352,
 19 1359 (Fed. Cir. 2000) (“Determining whether an accused process or device infringes a patent claim is a
 20 two-step process. The first step is claim construction, which involves ascertaining the scope and
 21 meaning of the claims at issue, while the second step involves determining whether the claims *as*
 22 *construed* read on the accused device.”) (emphasis added, quotations omitted); *TechSearch, L.L.C. v.*
 23 *Intel Corp.*, 286 F.3d 1360, 1369 (Fed. Cir. 2002) (summary judgment of noninfringement is proper
 24 “where the patent owner’s proof is deficient in meeting an essential part of the legal standard for
 25 infringement, because such failure will render all other facts immaterial.”).

26 **C. The Customer Defendants’ Inputs, As Required By The Design Compiler System,**
 27 **Are Not Architecture Independent.**

28 Ignoring Ricoh’s semantic games of whether or not the inputs are RTL, structural RTL,

functional RTL, or Darringer RTL, it is clear that there is no infringement simply because the inputs are not architecture independent. For each circuit element, the inputs, outputs, latches, clock, function, and a specification of how the outputs and latches are set based on the value of the inputs and the latches from the previous values of the latches for each clock cycle are included in the descriptions input into Design Compiler. Thus, the inputs for each circuit element are in fact architecture dependent. Casavant Decl. at ¶¶ 42-43.

Indeed, the 1991 Synopsys VHDL Reference concisely confirms that the HDL inputs to Design Compiler are decidedly “architecture dependent”:

The input to HDL synthesis is an RTL (register transfer level) functional description of the network to be implemented. RTL descriptions are distinct from behavioral level descriptions. The distinction is that *a behavioral description has no implied architecture in its representation, while an RTL level description has a definite, implied architecture.*

Ex. 21 at 3 (emphasis in original).

D. If Claim 13 Is Not Infringed, then Claims 14-17 Cannot Be Infringed.

Claims 14-17 are all dependent on claim 13. Ex. 1 '432 patent, 16:14-17:10. Thus, if the Court finds that claim 13 is not infringed, then claims 14-17 also are not infringed. *See Wahpeton Canvas Co., Inc. v. Frontier, Inc.*, 870 F.2d 1546, 1552 n.9 (Fed. Cir. 1989) (“One who does not infringe an independent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim.”).

1 **IV. CONCLUSION**

2 Based on the Court's interpretation of "architecture independent actions and conditions," the
 3 Customer Defendants' accused input descriptions cannot infringe the asserted claims of the '432
 4 patent. In addition, Ricoh's theory of infringement is critically flawed with respect to what Ricoh
 5 alleges are the "cell selection rules" within the Design Compiler system. Either of these flaws alone is
 6 sufficient to defeat Ricoh's infringement claims. The Court should therefore grant summary judgment
 7 of non-infringement in favor of the Customer Defendants on all of the asserted '432 patent claims.

8 Dated: August 18, 2006

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